Introduction to Integrated Circuit Technology

Third Edition

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IC KNOWLEDGE LLC

1.0. Introduction

At IC Knowledge, we have found a wide diversity in our clients and web site visitors with respect to their understanding of Integrated Circuit (IC) technology. Some of the people we interact with have a strong understanding of IC technology, but there is also a substantial group that purchases or uses the technology without a strong understanding. For the later group, we though it would be useful to produce a basic introduction to IC technology, and that is the objective of this publication.

We have written this publication assuming no more technical background than a high school education, and any technical terms will be defined when they are introduced. We have attempted to provide a good high level overview of the technology in this document, if you have questions about the content or would like to provide us with feedback, please e-mail us at info@icknowledge.com.

2.0. Basic electronic concepts

Electronic circuits regulate and control the flow of electric current. Electric current is the flow of electrons, the tiny subatomic particles that surround the nucleus of atoms. Electrons carry a fixed negative electric charge and the movement of electrons carries charge from one location to another - the flow of electrons is referred to as electric current. Electric current is driven by a difference in potential from one location to another measured in volts. Electric current flows easily through materials that are conductors, and is blocked by materials that are insulators. The amount of resistance that a material presents to the flow of electric current is logically called resistance. Conductors have low resistance to the flow of current and insulators have extremely high resistance (essentially infinite until the voltage is so high that the material breaks down). For a given voltage, the higher the resistance the less current that will flow and the lower the resistance the higher the current that will flow. Conversely, for a given resistance, the higher the voltage the more current that will flow and the lower the voltage the less current that will flow.

Basic Definitions

- Current - the flow of electrons carrying electric charge.
- Voltage - the force driving the flow of current.
- Resistance - a material's resistance to the flow of electric current.
- Conductor - a material that readily supports the flow of electric current.
- Insulator - a material that blocks the flow of electric current.

3.0. Electronic circuit elements

Electronic circuits are made up of a number of elements used to control current flow. There are a wide variety of different circuit elements, but for the purpose of this discussion the circuit elements will be restricted to the four most commonly used in ICs, these are, resistors, capacitors, diodes and transistors. Resistors, provide a fixed amount of resistance to current flow. Capacitors, store electric charge until discharged somewhat similar to a battery. Diodes, allow current to flow in one direction but not in the opposite direction, a one way valve. Transistors, provides two major modes of action, one, a switch turning current flow on and off, or two, act as an amplifier whereby an input current produces a larger output current.

An Integrated Circuit, or IC, is nothing more than a number of these components connected together as a circuit all formed on the same substrate.

IC Circuit Elements

- Resistors - resists current flow.
- Capacitors - stores charge.
- Diodes - allows current to flow in only one direction.
- Transistor - switches and or amplifies current.

4.0. What is a Semiconductor?

A semiconductor is a material that may act as a conductor or as an insulator depending on the conditions. Diodes and transistors are made with semiconductor material and resistors and capacitors may be made on or in semiconductor materials as well. As the scientific community began to understand semiconductor materials, the transistor and later the IC were invented (see "History of the IC" at www.icknowledge.com for more information). Resistors and capacitors as individual components are commonly made without the use of semiconductor materials but the ability to make them with semiconductor material made it possible to integrate them with diodes and transistors. Semiconductors may be made more conductive by adding other impurity elements to the semiconductor material and the ability to do this selectively, i.e., add impurities to one part of a semiconductor material and not to other parts is what enables IC fabrication to take place. Areas of semiconductor material that are highly pure and therefore have little or no impurities act as insulators. This is the key to IC fabrication and will be discussed further in the sections that follow.

5.0. Integrated Circuit Manufacturing Overview.

At the highest level, the manufacture of ICs may be broken up into 5 major steps - see figure 1.

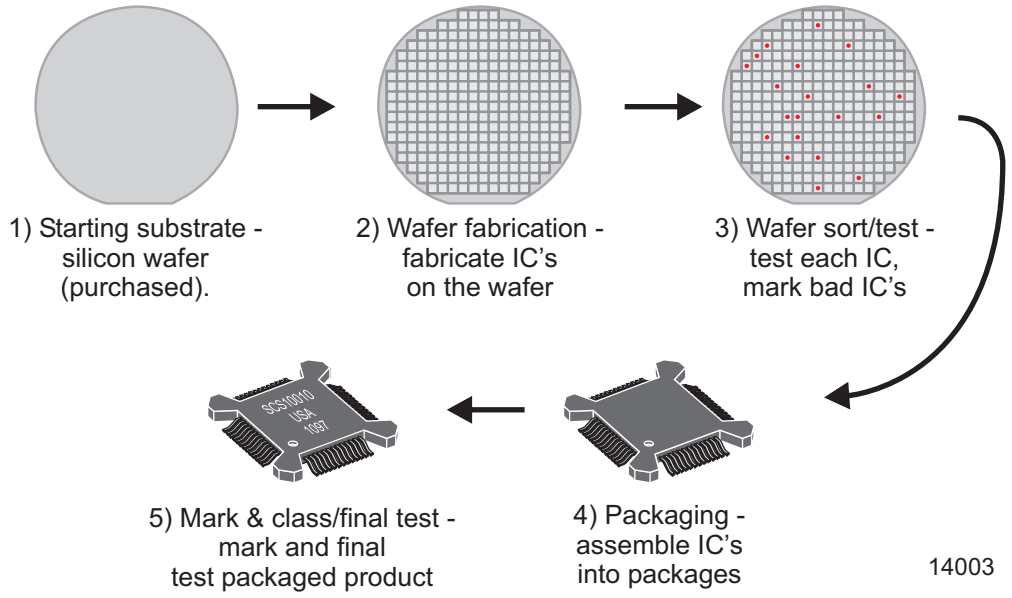


Figure 1. IC manufacturing.

The five major steps are:

1. Starting substrate - the starting substrate is purchased by virtually all major IC producers. Starting substrates will be discussed further in section 6.0.
2. Wafer fabrication - the process of fabricating a numbers of ICs on the surface of the wafer simultaneously. Wafer fabrication will be discussed further in section 8.0.
3. Wafer sort/test - each IC (referred to as a die) on the wafer surface is tested and the bad die are marked with an ink dot or in an electronic map. The bad die are discarded after the wafer is sawn up for packaging to save the cost of packaging bad die. Wafer test will be discussed further in section 10.0.
4. Packaging - the wafer is sawn up into individual die and the good die are assembled into protective packages. Packaging will be discussed further in section 11.0
5. Mark and class/final test - in order to insure that the die were not damaged during packaging, the packaged product is tested and marked with the product type. Final test will be discussed further in section 12.0.

6.0. Silicon Wafers

Far and away the most common material for IC fabrication is silicon (there are other materials in use, but only for small niche applications). Silicon is an abundant material in the earth's crust and relatively easy to obtain and refine. Silicon is a semiconductor, although silicon has become the dominant IC material not so much because it is a great semiconductor material, but rather because it is relatively easy to work with.

The silicon used for IC fabrication has been highly purified, grown into nearly perfect crystals and sliced up into discs, called wafers, less than a millimeter (mm) thick and anywhere from 100mm (4") to 300mm (12") in diameter (smaller sizes were used early in the development of the industry but are now rarely used in production). Silicon wafers are highly polished - appearing mirror like, extremely flat, and extremely clean and particle free at the start of fabrication.

100mm (4"), 125mm (5") and 150mm (6") wafers typically have a flat section ground onto one or more edge to mark how the crystal planes are oriented in the wafer and allow consistent alignment of various layers built up on the wafer - see figure 2a. 200mm (8") and 300mm (12" wafers use a small notch in place of a flat because a flat takes away an unacceptable amount of wafer area on the larger wafers - see figure 2b.

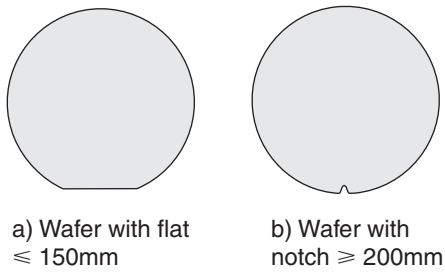


Figure 2. Silicon wafer orientation indications.

Silicon wafers were at one time internally manufactured by the IC companies who then fabricated circuits on them, but now virtually all IC manufacturers purchase the wafers from a third party.

There are three major types of silicon wafers currently in use for IC fabrication:

- Raw wafers, silicon wafers without any additional processing. For state-of-the-art ICs raw wafers are mainly used for DRAMs.

Wafer Types

- Raw - basic wafer used to make ICs.
- Epitaxial (Epi) - a raw wafer with a single crystal film deposited on it.
- Silicon On Insulator (SOI) - a thin single crystal silicon film on an insulating

- Epitaxial wafers, silicon wafers with a single crystal silicon layer deposited on them. The deposited layer typically has different properties than the underlying raw wafer. Epitaxial layers allow the properties of the layer in which the devices are formed to be more tailored than in a raw wafer and are nearly universal for the latest state-of-the-art Logic ICs. Epitaxial wafer costs are 1.4 to 2.5 times the cost of a raw wafer.
- Silicon on Insulator (SOI) wafers - silicon wafers upon which an insulating layer is formed with a thin single crystal silicon layer on top of the insulating layer. SOI wafers reduce the amount of power drawn by an IC when the circuit is switching at a high speed. SOI wafers costs are 4 to 15 times the cost of a raw wafer. SOI is primarily used in low power and some high performance applications. We expect the use of SOI to increase and even become mainstream as linewidths continue to shrink.

Figure 3 illustrates the basic wafer manufacturing process.

The process steps are:

- Pull crystal ingot - a small seed of single crystal silicon is dipped into a crucible of molten silicon. The crucible and seed are rotated in opposite directions and the seed is slowly withdrawn from the crucible (figure 3a).
- Ingot grind - the silicon crystal ingot is ground to create a consistent diameter for the whole ingot (figure 3b).
- Saw off ingot ends - the two ends of the silicon ingot will not be usable and are sawn off using a diamond saw (figure 3c).
- Saw up the ingot into wafers - the Ingot is sawn up into wafers each approximately 1/2mm to 3/4mm in thickness (100mm to 300mm wafers)(figure 3d).
- Edge grind wafers - the edges of the wafers are ground to round off the sharp edges. Edge grinding minimizes chipping of the wafer edges during subsequent processing (figure 3e).
- Lap wafers - a process called lapping is used to flatten out the wafers and ensures the two wafer faces are parallel (figure 3f).
- Damage removal etch - a special wet etch is used to etch off the surface damage left from lapping (figure 3g).
- Polish - the polish step removes the final residual damage layer on the wafers and creates a mirror polish surface (figure 3h).

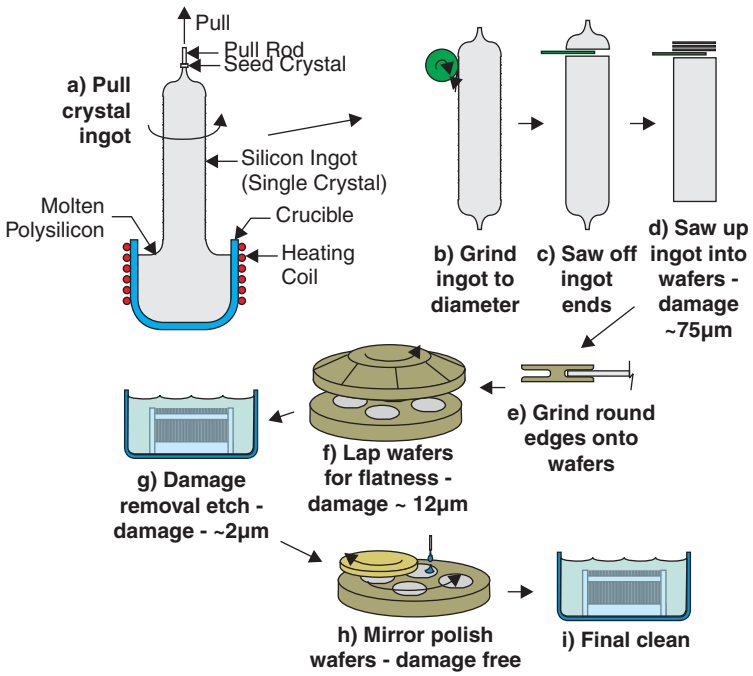


Figure 3. Silicon wafer manufacturing process.

- Final clean - the final clean step removes any contaminants left on the wafer surface from the previous steps (figure 3i).

The resulting wafer is a highly pure - nearly perfect single crystal, with crystal planes precisely oriented to the wafer surface.

7.0. How small is small?

Before delving into wafer fabrication - the fabrication of incredibly tiny IC elements, it is useful to review the size scale of the circuit elements being discussed. The units of measure utilized in this publication are defined in table 1..

Table 1. Units of size

Unit	Symbol	Relationship
Meter	m	---
Millimeter	mm	One thousand millimeters equals one meter.
Micrometer, also called a micron	μm	One million micrometers equals one meter, one thousand micrometers equals one millimeter.
Nanometer	nm	One billion nanometers equals one meter, one thousand nanometers equals one micrometer.
Picometer	pm	one trillion picometers eqauls one meter and one thousand picometers equals one nanometer.

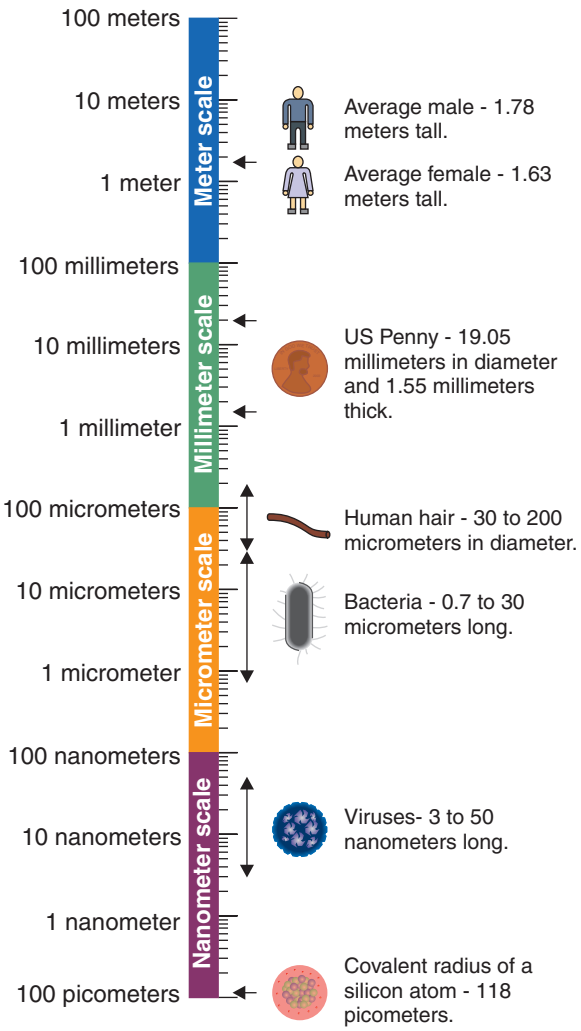


Figure 4. Size scale

Once the units are defined, the size of some common objects may be put in perspective, see figure 4.

The average height of people is measured in meters, at teh millimeter scale is the diameter and thicknes sof a penyy and at the micrometer scale is the thickness of a human haidr and size of bacteria, viruses are nanometer scale in size and finally atoms are picometers in size.

The smallest processes currently in production are 90nm processes and some of these processes actually have features as small as 50nm. From figure 4, 50nm may be put into perspective relative to some common objects. 50nm is slightly larger than a large virus and much smaller than bacteria.

8.0. Wafer fabrication

IC's may have anywhere from a few components to >1 billion transistors and 1 billion capacitors integrated together on the latest 1Gb DRAM's. Depending on the wafer size and IC complexity, there may be anywhere between tens and tens of thousands of die on a wafer. The key to successfully fabricating all of these components on one substrate is the ability to selectively change the properties of silicon. In the next several sections, the key technologies behind wafer fabrication will be described.

8.1. Cleaning

The cleanliness of wafers during processing is so critical that every wafer is cleaned prior to any high temperature or deposition step. Complex sequences of acid and alkali solution are utilized to remove particles, organic films, metals and any pre-existing "native" oxide films. The most commonly used clean in the industry is the RCA clean (see sidebar).

RCA Clean

- The most commonly used clean - the RCA clean includes multiple steps:
- SC1 (standard clean 1) - removes organic films and particles.
- SC2 (standard clean 2) - removes metals.
- HF (hydrofluoric acid) removes silicon dioxide layers.
- May include SPM (sulfuric peroxide) - removes gross organic layers.

8.2. Oxidation

One of the key reasons that silicon is the most commonly used semiconductor, is that it is easy to work with and one of the key factors in making silicon so easy to work with is the ability to grow a high quality insulating layer on silicon. If silicon is exposed to oxygen or water vapor at high temperatures, oxygen combines with silicon to form silicon dioxide, a glass. Silicon dioxide is stable at high temperatures, an excellent barrier and an excellent insulator; figure 5 illustrates the basic silicon oxidation process.

Silicon oxidation

- Silicon (Si) combines with oxygen (O_2) at high temperature to form silicon dioxide glass (SiO_2).

$$Si + O_2 \rightarrow SiO_2 \qquad (1)$$

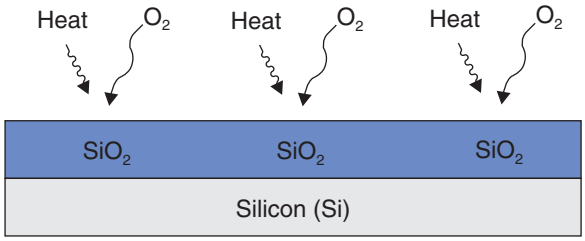


Figure 5. Silicon oxidation.

8.3. Photolithography

At the heart of wafer fabrication technologies is photolithography. Photolithography defines the patterns that when used in conjunction with etching can pattern deposited and grown thin films, and combined with ion implantation can selectively change the properties of silicon. Photolithography creates patterns in photoresist - a liquid photosensitive chemical that resists etching processes.

The photolithography process works as follows:

- Surface prime - a surface treatment to drive off moisture and improve adhesion of photoresist, typically accomplished by heating the wafer in a primer chemical vapor.
- Coat - a small amount of photoresist (a few milliliters) is dispensed onto the center of the wafer and then spun at high speed to produce a uniform thin film - see figure 6

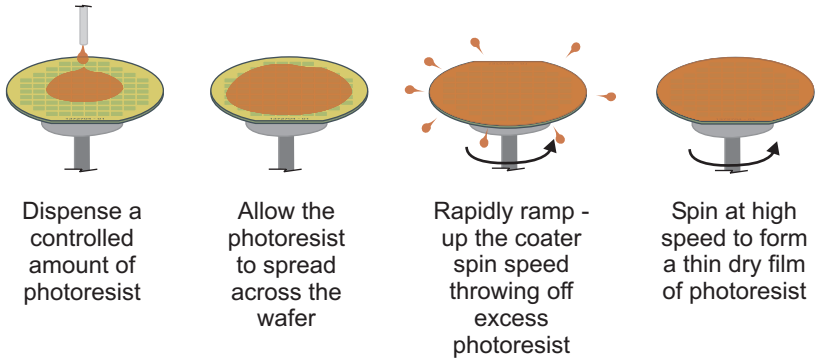


Figure 6. Photoresist coating process.

- Pre-bake - photoresist contains a solvent used to keep the polymer and photo sensitive chemical in suspension. Once the photoresist is coated onto the wafer, the solvent is driven off by a pre-bake to stabilize the film.
- Exposure - the exposure step photographically transfers a pattern from a reticle to the photoresist coating on the wafer surface. Reticles are glass plates with patterns of opaque and transparent areas. A reticle will typically have the patterns for a few die on it and will be stepped across the wafer exposing the pattern after each step to cover the wafer with patterns. In order to ease the task of reticle fabrication and make the process less defect sensitive, reticle patterns are either 5x or 4x the size of the desired feature on the wafer, and the reticle pattern is optically shrunk before reaching the wafer. Figure 7 illustrates pattern formation on a wafer by photolithography.
- Post exposure bake - the latest exposure tools use very short wavelength - deep ultraviolet light (DUV) to enhance resolution. Photoresist for DUV are chemically amplified and require a bake step after exposure to complete the chemical reaction initiated by exposure.
- Develop - the effect of the developing step depends on the type of photoresist being used. For positive photoresist the developer dissolves areas exposed to light more quickly and dissolves areas where the light was blocked more slowly. For negative photoresist the developer dissolves the areas not exposed to light more quickly and areas exposed to light more slowly. The

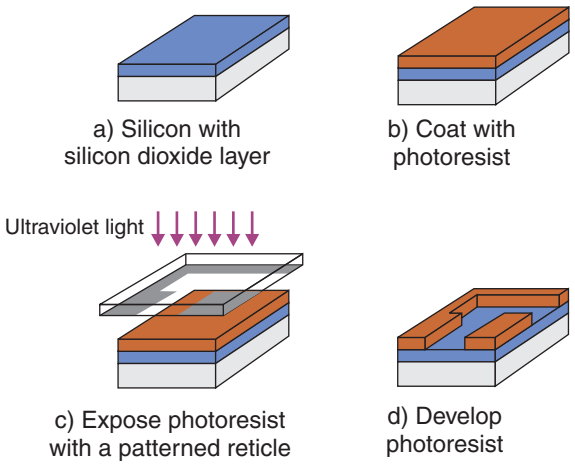


Figure 7. Photolithography process.

end result is that for a well designed process, at the end of the develop step the pattern from the reticle is replicated in the photoresist.

- Post bake - prior to developing, bake temperatures must be kept low enough to not break down the photosensitive chemical in the photoresist. Following the develop step this is no longer a consideration and higher temperature bakes are used to stabilize the film prior to subsequent processing.

Following the photolithography process the photoresist pattern may be used to create selective processing, for example an etch that etches an underlying film but does not etch photoresist. Following etching the photoresist pattern would then be stripped off and the wafers sent on for further processing that might include further photolithography steps.

Photolithography

- Prime - coat the surface with an adhesion promoter.
- Coat - coat the wafer with a photosensitive liquid - photoresist.
- Soft Bake - bake the photoresist to dry it without breaking down the photosensitive chemical.
- Expose - expose the photoresist to ultraviolet light through a patterned reticle transferring the reticle pattern into the photoresist.
- Post Exposure Bake - certain types of photoresist require a bake after exposure to complete the exposure reaction.
- Develop - wash away the photoresist wherever light exposed a pattern into the photoresist and leave the photoresist wherever the light was blocked.
- Post Bake - bake the photoresist to stabilize the film prior to subsequent processing. The photoresist no longer needs to be light sensitive so higher temperatures than soft bake may be used.

8.4. Ion Implantation

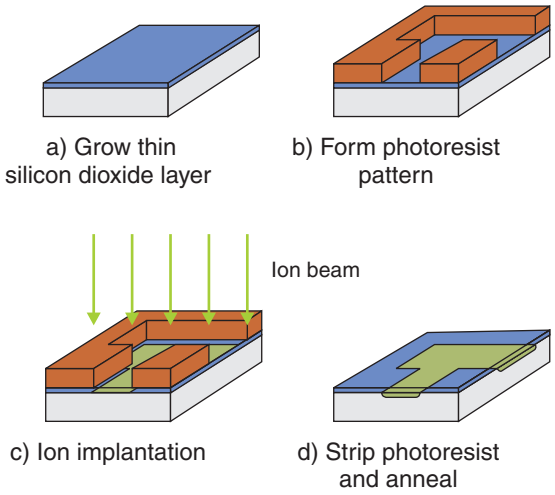


Figure 8. Ion Implantation.

As was previously discussed, impurities may be used to change the electrical properties of silicon. Introducing impurities into silicon in a controlled manner is the key to forming integrated circuits. Ion Implantation is currently the most common method for introducing impurities into silicon wafers. In an ion implanter, impurities to be introduced into silicon are ionized, i.e. stripped of one or more electrons giving the impurity ion a positive charge. A high voltage electric field is then used to accelerate the ions to a very high energy. This acceleration process is done in a vacuum so that the ions don't collide with any gases during acceleration. The accelerated ions are then "implanted" into the silicon surface by virtue of their high energy causing them to penetrate the surface they are aimed at before coming to rest.

Ion Implantation

- Impurities with an electric charge are accelerated to high energy and shot into the wafer surface.

The Ion Implantation process is made selective by using a photoresist pattern to block impurity ions from reaching silicon where no impurities are desired. The selective introduction of impurities process begins with the growth of a thin silicon dioxide layer. The silicon dioxide layer protects the silicon surface, but must be thin enough not to block the implanted ions. Photoresist is then applied and patterned as outlined in figure 7, and ion implantation is performed. Following ion implantation, the photoresist is stripped off and a high temperature furnace process is used to anneal out the damage from the high energy ions impacting the silicon - see figure 8.

8.5. Etching

In the following sections a variety of thin film deposition techniques and thin films will be described. Whenever a thin film is patterned in IC technology, some form of etching step is always involved, this even includes techniques such as damascene and dual damascene.

Early in the development of IC technology all etches were based on liquid chemicals (wet etching). In most cases wet etching - etches in all directions at the same rate (isotropic etch). The result of this is that while etching down through a film, the etchant is also etching underneath the edge of the photoresist - see the left side of figure 9. More recently etching processes have used excited gas molecules to performing etching and can achieve faster etching in one direction than in other directions (anisotropic etching) -see the right side of figure 9.

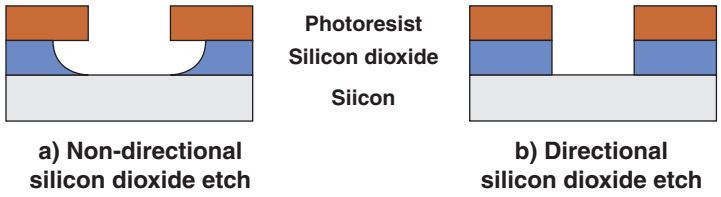


Figure 9. Isotropic versus anisotropic etching.

When linewidths were relatively large, isotropic etching was acceptable, but as linewidths shrink isotropic etching can result in complete undercutting of the feature being printed - see figure 10. Notice how the right most line is almost completely undercut away.

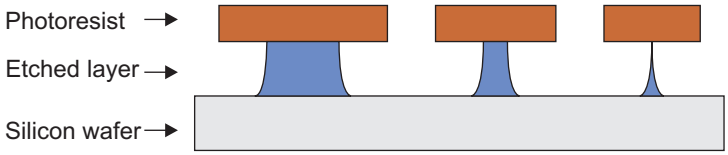


Figure 10. Isotropic etching versus linewidth.

In addition to undercutting problems from wet etches, as IC technology advanced new materials such as polysilicon and silicon nitride could either not be wet etched or could not be etched with etchants that are compatible with photoresist. In current state-of-the-art processes, wet etching has been almost completely supplanted by dry etching.

Dry etching processes use a variety of halogen containing gases such as fluorine, chlorine and bromine compounds. High frequency energy is used to split up the gas molecules in a low pressure chamber creating highly reactive products. The chemically active etch products may be combined with chemistries to produce polymers and ions to create anisotropic etches.

8.6. Chemical Vapor Deposition (CVD)

In CVD processes, gases or chemical vapors are reacted to form a deposited film, most commonly at low pressure. Reactions may be induced by heat as in CVD, high frequency energy as in Plasma Enhanced CVD (PECVD) or light as in Photon Assisted CVD (PHCVD). If the chemicals being used in the reaction are made up of molecules combining metals and organics, then the CVD process is referred to as Metal Organic CVD (MOCVD). There is also Low Pressure CVD (LPCVD) and Sub Atmospheric CVD (SACVD).

An example of a CVD process is illustrated in figure 11.

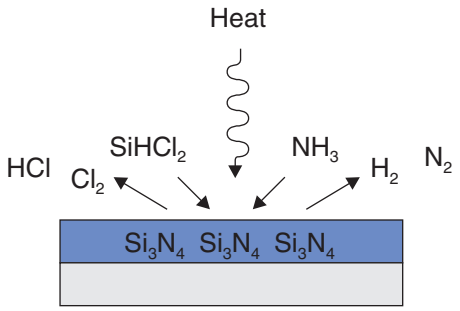


Figure 11. CVD process.

Etching

- Wet etching uses liquid chemicals, primarily acids to etch materials. Wet etching is predominantly non-directional.
- Dry etching uses gases in an excited state to etch materials. Dry etching may be non-directional or directional.
- Isotropic - etches at the same rate in all directions.
- Anisotropic - etches in one direction faster than other directions.

In figure 11, ammonia gas (NH_3), and dichlorosilane ($SiHCl_2$), are reacted to produce a deposited solid film of silicon nitride (Si_3N_4), and gaseous by products that are pumped away-hydrogen chloride (HCl), chlorine Cl_2, hydrogen (H_2) and nitrogen (N_2). Some of the films used in IC fabrication that are typically deposited by CVD are listed in table 2.

Table 2. IC thin films commonly deposited by CVD

Film name	Chemical formula
Silicon dioxide	SiO_2
Silicon oxynitride	SiO_xN_y
Silicon nitride	Si_3N_4
Polysilicon	Si
Titanium nitride	TiN
Tungsten	W
Fluorinated Silicon Glass (low-k)	SiO_xF_y
Hydrogen and carbon doped oxide films (low-k).	

8.7. Sputter Deposition

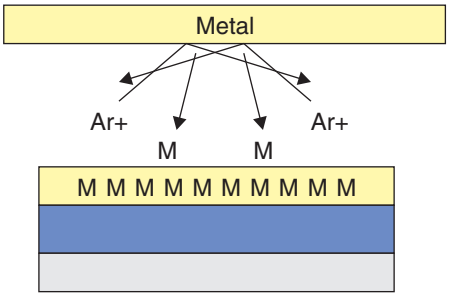


Figure 12. Sputter process.

Many metal films used in IC fabrication are deposited by sputtering. In the sputtering process, argon gas is excited by a high energy field to split up into positively charged argon ions and free electrons. An electric field attracts the argon ions toward a target made out of the material to be deposited. The argon ions physically knock loose atoms of the target material that then deposit out onto the wafer surface. Although CVD generally covers steps better than sputtering, not all metals may be deposited by CVD. Figure 12 illustrates the sputtering process

Thin Films

- Grown or deposited films a few microns to a few nanometers thick.
- Common films include:
- Silicon Dioxide - insulator.
- Silicon Nitride - protects the finished IC.
- Polysilicon - used as a conductor and a control electrode for certain types of transistors.
- Aluminum - used as a conductor.
- Copper - the newest type of conductor, has lower resistance than aluminum.
- Titanium Nitride or Tantalum Nitride - used as a barrier between films to prevent interactions.

8.8. Chemical Mechanical Planarization

As IC technology developed, more and more metal layers have been required to provide interconnect with acceptable signal delays. As more and more metal layers are stacked up, topography becomes an overwhelming issue. CMP combines chemical and mechanical material removal to produce fully planar surfaces. The CMP process is illustrated in figure 13.

tThe exact mechanism of CMP depends on the material being polished and the polishing slurry used, but generally speaking a chemical reaction is used to soften up the film being removed and then mechanical abrasion from the slurry particles removes the material. The advantage of CMP over a purely mechanical process is that the chemicals used to perform the softening function can be tailored to attack only specific materials so that the removal rate is relatively high for one material and relatively low for other materials. The difference in removal rates between materials allows a polishing stop layer to be used in some cases.

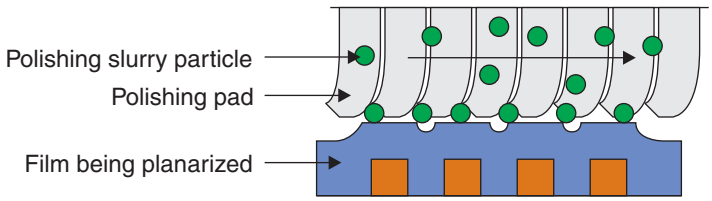


Figure 13. Chemical mechanical planarization.

8.9. Putting it all together

The unit steps described above are combined with other unit steps into complex process flows with hundreds of steps where 20 to 30 or more reticles are used to print patterns onto wafers. The end result is a number of ICs on a single wafer, that depending on the wafer size and the size of the IC may number, tens, hundreds, thousands or ten of thousands of ICs. Each IC may have tens of millions or even over a hundred million circuit elements.

Memory ICs now in production have over 1 billion transistors and 1 billions capacitors on a single IC. Microprocessors have reached tens of millions of transistors per die. The left side of figure 14 illustrates a technician holding a 300mm wafer and the right side illustrates an enlarged photograph of one Pentium 4™ IC. The IC illustrated in figure 14 contains over 42 million transistors in an area smaller than the surface of a dime and there are approximately 281 of these ICs on a 300mm wafer.

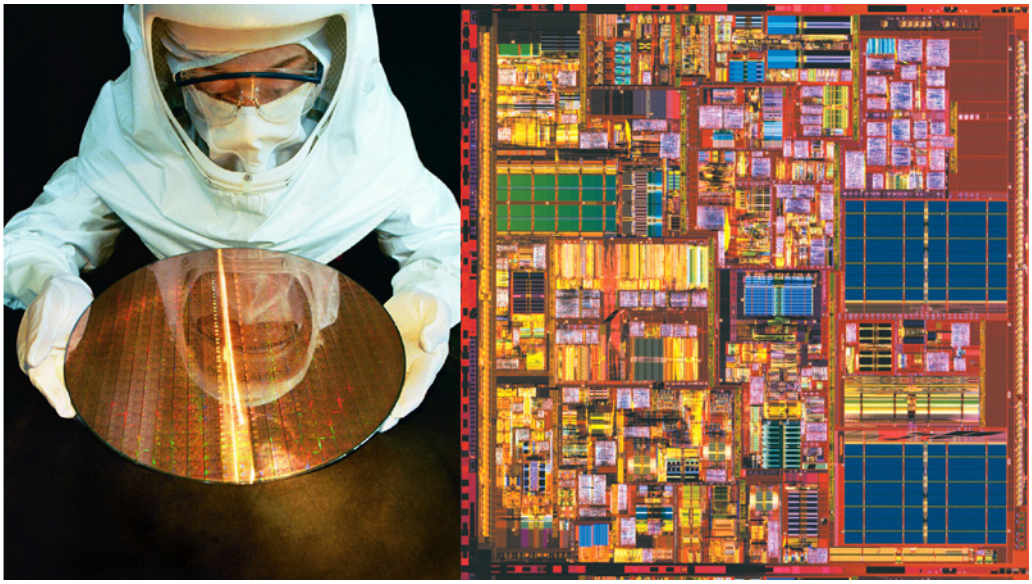


Figure 14. 300mm wafer and Pentium 4™ IC. Photos courtesy of Intel.

9.0. Cleanliness and Yield

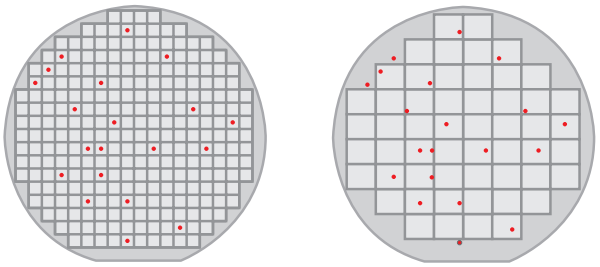


Figure 15. Defect density and yield concept.

During processing, ICs are very susceptible to any kind of small particle or defect landing on the surface of the IC. ICs in wafer form are referred to as die. Experience has shown that particles 1/2 to 1/3 the size of the smallest feature on an IC can "kill" the die - referred to as a killer defect. For 90nm processing, particles 30 to 45nm in size can kill the circuit, and measurements of atmospheric air have found that there are millions of particles that size or larger in a cubic foot of air. The mechanics of particle deposition from air are quite complex, but

suffice it to say that with millions of particles floating around, the likelihood of a killer defect landing on a given die is very high. The number of killer defects is characterized by the defect density on the wafer surface given in defects per unit area. The resulting yield depends on the size of the die and the defect density. Actual yield calculations require yield probability models, but the basic concept is illustrated in figure 15. On the left side of figure 15, a wafer is shown with a defect pattern of 20 defects and a relatively small die that results in 264 die per wafer. The number of die without defects is 244 and the resulting yield is 92%. On the right side of the figure a wafer is shown with the same defect pattern, but a larger die. There are 54 die per wafer of which 38 die have no defect resulting in a 70% yield!

As ICs have developed, the desire to pack more functionality onto individual ICs has driven linewidths to ever smaller sizes - see figure 16, and ICs have simultaneously gotten larger - see figure 17. The net result is that lower particle levels are required for good yield, and the size of particles that can kill a circuit is also shrinking, requiring ever increasing cleanliness levels.

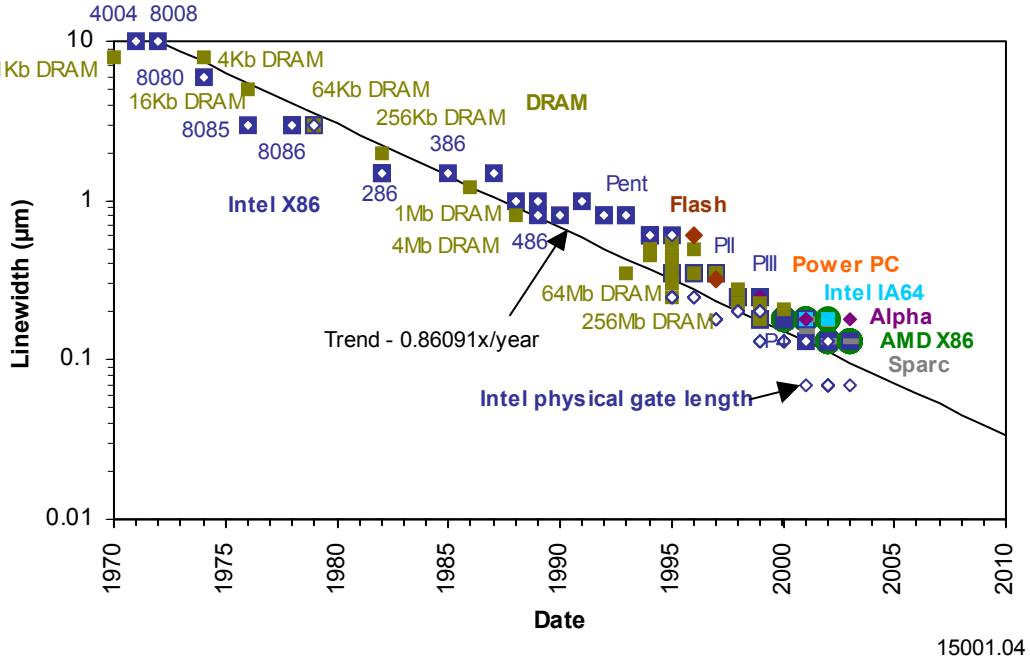


Figure 16. Linewidth trends.

In order to meet the cleanliness requirements and manufacture ICs with high yield, cleanrooms are used. Cleanrooms are rooms with continuous circulation of air out of the room, through a high quality HEPA or ULPA filter and back into the room - continuously sweeping particles out of the room.

Figure 18 illustrates a simple cleanroom. Cleanrooms used for IC production have the filters located in the ceiling and the air flows down the room to or near the floor before exiting the room. The down flow or vertical style of cleanroom keeps the dirtiest air down near the floor where no work is exposed and has the benefit of gravity aiding in particle removal.The quality of cleanrooms is defined by federal standard 209E. Under 209E, a cleanroom with less than 100 particles per cubic foot larger than 0.5µm is a Class 100 cleanroom, or less than 10 particles per cubic foot

greater than 0.5µm is class 10, and so on. High yield on current state-of-the-art ICs requires better than Class 1 cleanrooms.

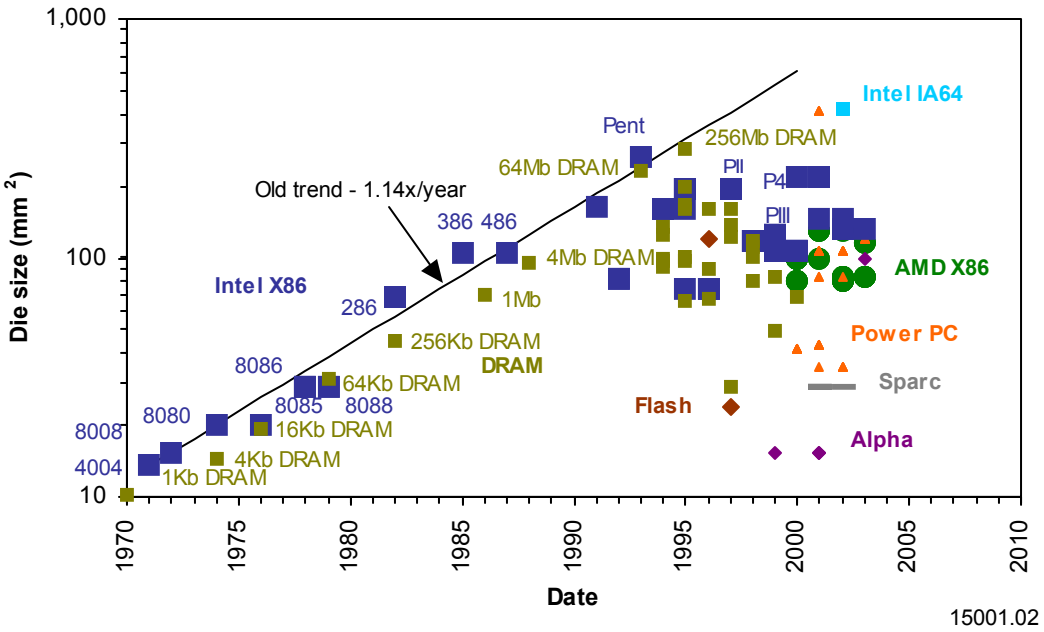


Figure 17. Die size trends.

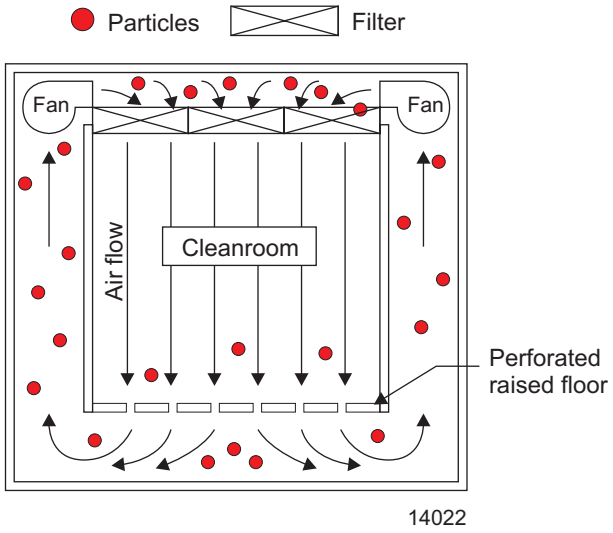


Figure 18. Basic cleanroom configuration.

Water, chemicals and gases utilized in the manufacturing process must also be low in particles and free of contaminants down to the parts-per-billion or even parts-per-trillion range.

10.0. Wafer Test

Upon completion of wafer fabrication, not all of the die on a wafer will be fully functional. The yield loss at this step ranges from a few percent for mature processes, to 90% or more for new processes. In order to avoid adding additional value to defective units during packaging, a 100% test of the die is performed.

Each die that has been fabricated on the wafer has a series of pads referred to as bond pads where connections will be made to the die during assembly. The die is covered with a protective passivation layer everywhere except where the pads are located. For each type of die being tested a specialized "probe card" is fabricated with a set of tiny needles spaced apart so they line up with the bond pad openings - see figure 19.

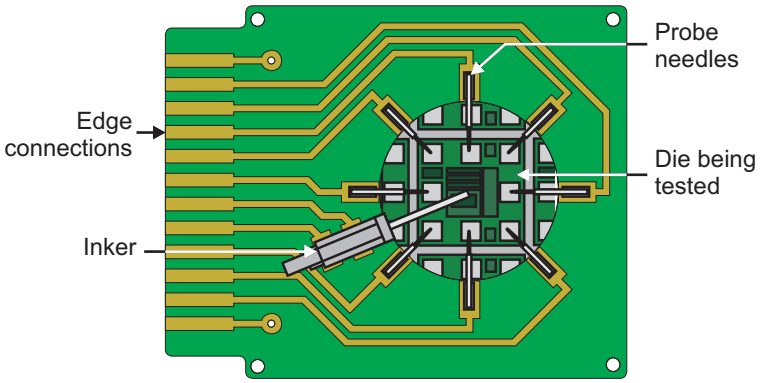


Figure 19. Simple probe card.

The wafer to be tested is held onto a chuck in a piece of equipment referred to as a wafer prober - figure 20b. The prober also holds the probe card and mechanically positions the probe card needles over the bond pads on a die, touches the needle down to make an electrical connection for testing, and following testing lifts the needles and positions them over the next die.

The wafer prober is connected to a tester, an automated piece of equipment that performs electrical tests on each die - see figure 20a. The tester is basically a computer and some power supplies, meters and function generators that can be programmed to perform a variety of electrical measurements. The tester communicates with the prober telling the prober when each die has been tested and whether the die is good or not. When a die tests "bad", a tiny ink dot may be dispensed onto the die to mark it bad or an entry may be made in an electronic map to denote the location of the bad die.

Cleanroom concepts

- Cleanroom - a room with continuos circulation of filtered air.
- Vertical cleanroom - a cleanroom with air flow from ceiling to floor - virtually universal for IC production.
- Cleanroom class - specifies the maximum number of particles greater than or equal to 0.5µm in size. Class 10 has less than 10, Class 1 has less than 1, etc.
- HEPA filter - high efficiency particle air - blocks 99.97% of particles >0.3µm.
- ULPA filter - ultra low particle air - blocks 99.999% of particles >0.12µm.
- Raised floor - a type of floor used in most Class 10 or better cleanrooms. The floor is perforated to allow air to flow down through the floor. An under-floor air plenum is used to return the air up to fans and filters for recirculation back into the ceiling of the room.

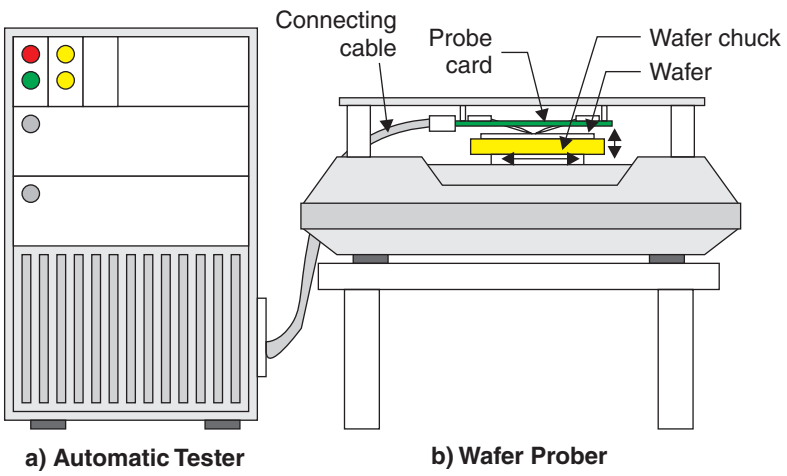


Figure 20. Wafer test set-up.

Wafer Test Terminology

- Probe card - a card with tiny needles used to make electrical connections to IC die being tested.
- Bond pad - pads on the die where electrical connection may be made.
- Tester - a computer controlled system that performs electrical tests automatically.
- Prober - a piece of equipment that holds the probe card and wafer being tested and steps the card across the wafer contacting each die. Operates under control of the tester.

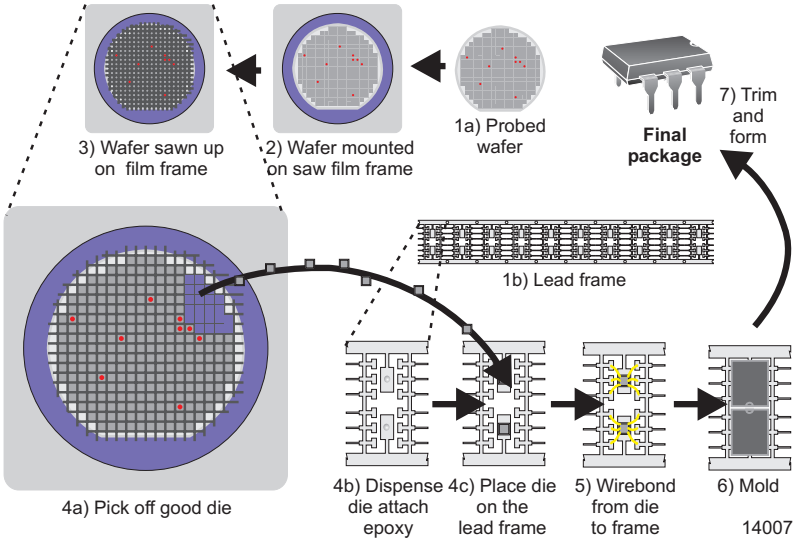
11.0. Packaging

Silicon ICs in “die” form are difficult to handle, fragile even though they have a protective layer, and the tiny bond pads are difficult to connect to. In order to further protect the die and make the parts easier to handle and connect, packaging is performed.

Historically, the most common packing method is as follows.

- After wafer test, the wafer is mounted onto sticky tape stretched over a metal frame. The backside - non circuit side of the wafer is stuck to the tape. An automated - high speed saw with a very thin diamond blade is used to saw apart the die. There is an area between each die that has no circuitry referred to as a street so that sawing does not damage the IC circuitry. The sticky tape serves to hold the individual die in place after sawing, see figure 21 - 1a through 3.
- Each good die on the wafer is now removed from the sticky tape and placed onto a metal frame referred to as a leadframe. This operation is performed by automated pick and place machines. The leadframe is etched or stamped into a pattern that will later become the electrical connection pins that protrude from the package. The leadframe also includes a pad that the die is epoxy mounted to, see figure 21 - 4a through 4c.
- Tiny wires, typically gold, are now attached from each bond pad down to a corresponding leadframe pin. This is the electrical connections from the die to the pins that eventually connects the die to the outside world. Wire bonding is also performed by automated systems referred to as wire bonders, see figure 21 - 5.
- A rectangular area of black epoxy is now molded around the die and leadframe leaving the leadframe pins sticking out. Molding is accomplished in large presses under heat and pressure, see figure 21 - 6.
- A mechanical tool now punches out each individual packaged IC from the leadframe bars that held the units in rows. The tool also bends the leads forming them into their final configuration.

- The units are branded with a part number, company name, date, etc. on the epoxy plastic to identify the part.



Packaging Flow

- Saw up the wafer into individual die.
- Mount the die down onto a leadframe.
- Wirebond from the die bond-pads to the leadframe.
- Mold epoxy around the die to protect it.
- Trim and form to break the individual packaged ICs apart.
- Mark the packages.

Figure 21. Plastic packaging process.

Figure 22 illustrates the common package styles and their popularity.

Recently, newer techniques have been developed to produce smaller packages and also enable higher frequency connections to ICs. The relatively large pins used to connect plastic packages to the outside world degrade high frequency signals. The newer techniques are generically referred to as "chip scale" packaging, the idea being that the "package" is barely any bigger than the silicon chip. One technique is called flip chip.

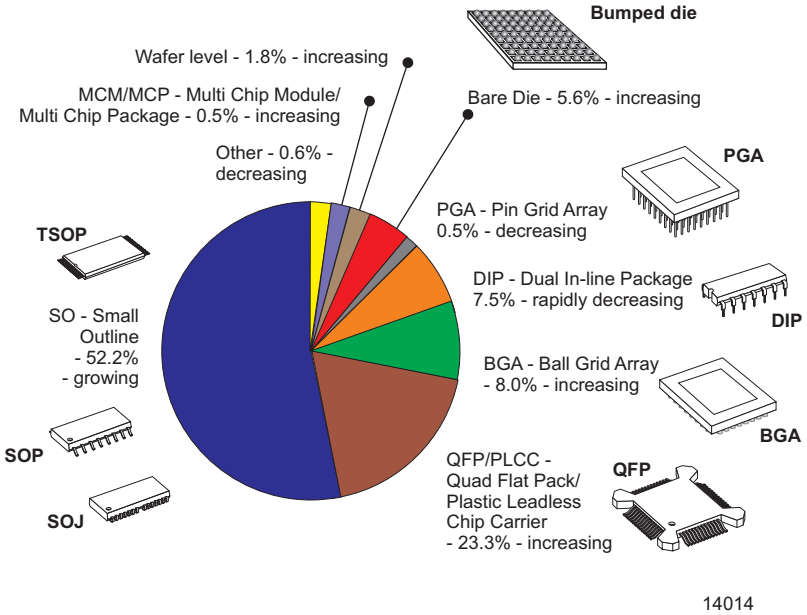


Figure 22. 2003 package types and market share.

In flip chip processing, tiny solder balls are fabricated on the bond pads, the silicon chip is then flipped over and soldered down to connecting pads on a substrate. The technique is compatible with high frequency, less expensive than wire bonding for high connections counts, and results in a very small "package". Additionally, for wire bonding, pads need to be at or near the edge of the IC to minimize wire length. In some cases the number of pads required for electrical connections exceeds the number

that will fit around the periphery of the IC. The IC size must be increased just to accommodate pads increasing the IC size and cost. With a flip chip approach pads can be placed in an array anywhere on the IC - see figure 23.

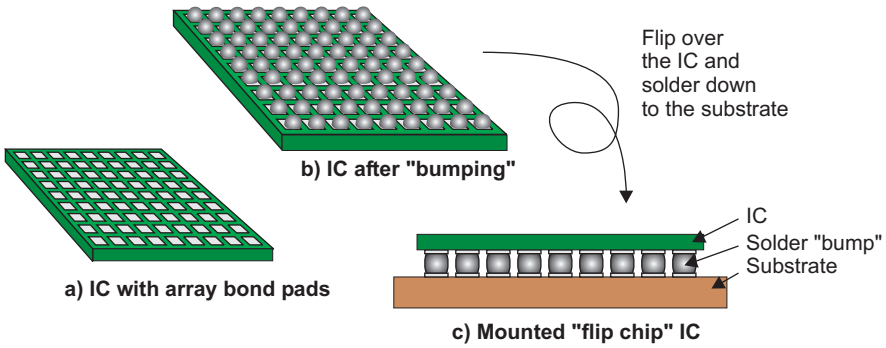


Figure 23. Flip chip process

Chip Scale Packaging

- Bare die are also sometime referred to as chip scale packing - the package is no bigger than the silicon chip (die)

12.0. Final Test

During the packaging process, die may be damaged or packaging may not be correctly performed. The defects introduced during packaging typically cause 1 percent or more of ICs to fail. Most customers today expect that only a few ICs per million will be non functional on arrival. Final test is a 100% test performed on each packaged IC prior to shipment to insure that any ICs improperly packaged are not shipped. Final test is similar to wafer test except a handler is used to “handle” the IC packages and make connections - see figure 24b. The handler is connected to a tester similar or identical to the one used at wafer test - see figure 24a.

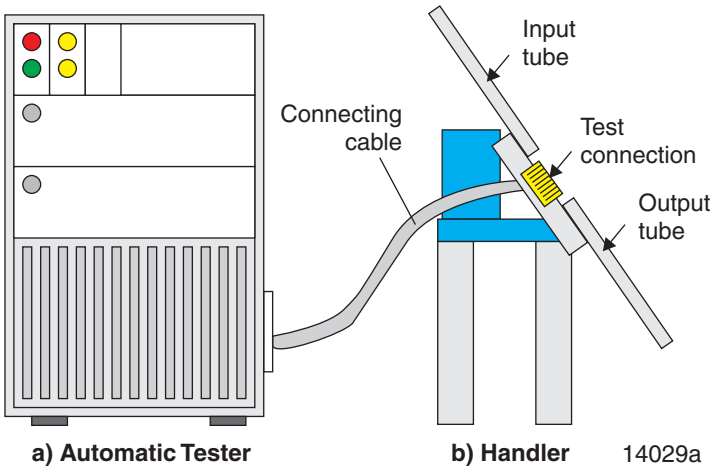


Figure 24. Final test system.

Final Test Terminology

- Tester - a computer controlled system that performs electrical tests automatically.
- Handler - a piece of equipment that moves parts from an input bin, makes electrical connection to the parts for testing, and then moves the parts to a output bin or bins. Operates under control of the tester.
- Binning - the practice of sorting parts based on some measured performance parameter.

At this point defective units are discarded and good units are ready for shipment. Many handlers provide “bins” for good and bad parts and may also provide additional bins so parts can be graded by speed of operation or other criteria. It is quite common to bin out parts at final test by grade. A common example would be Pentium microprocessors. One process flow produces processors that are then tested and sold as various speed grades. The highest speed grades are the rarest - highest performing parts and therefore have the highest selling price. The variations in spped are due to process variations across a wafer and wafer to wafer that occur during wafer processing.

13.0. Conclusion

In conclusion, IC technology relies on the ability of semiconductor materials to behave as conductors or insulators depending on impurities selectively added to the semiconductor. The process of producing an IC is made up of:

- A starting substrate - typically purchased.
- Wafer fabrication - fabricates the IC - die, on the wafer surface.
- Wafer test - tests each die.
- Packaging - packages the die for easy handling and protection.
- Final test - tests the packaged IC.

We hope you have found this publication interesting and informative. Once again we would like to encourage you to give us feedback, good or bad about content, depth of treatment or how understandable our explanations are. You may contact us by e-mail at info@icknowledge.com. There are also a variety of other resources available at ICknowledge.com (click on any of the underlined blue text to go there) including an extensive glossary of IC terminology and a history of the development of the IC. More advanced versions of this publication are available on a paid basis. Our brand new 2003 IC technology report covers IC Technology in a more complete manner with all of the very latest technologies at a level similar to this publication. Lattice Press has recently released Microchip Manufacturing an introductory level text book. This is the first full color text book on IC Technology and is available through our web site.

IC Knowledge.com: other suggested reading

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